PSoC® Creator™
Project Datasheet for 2020TPCApp1

Creation Time: 11/02/2020 16:11:23
User: WIN-VIRTUALBOX\Kearney
Project: 2020TPCApp1
Tool: PSoC Creator 4.4

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Table of Contents

1 Overview

The Cypress PSoC 6 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M4 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 63 series member PSoC 6 device. For details on all the systems listed above, please refer to the PSoC 6 Technical Reference Manual .

Figure 1. PSoC 63 Device Series Block Diagram

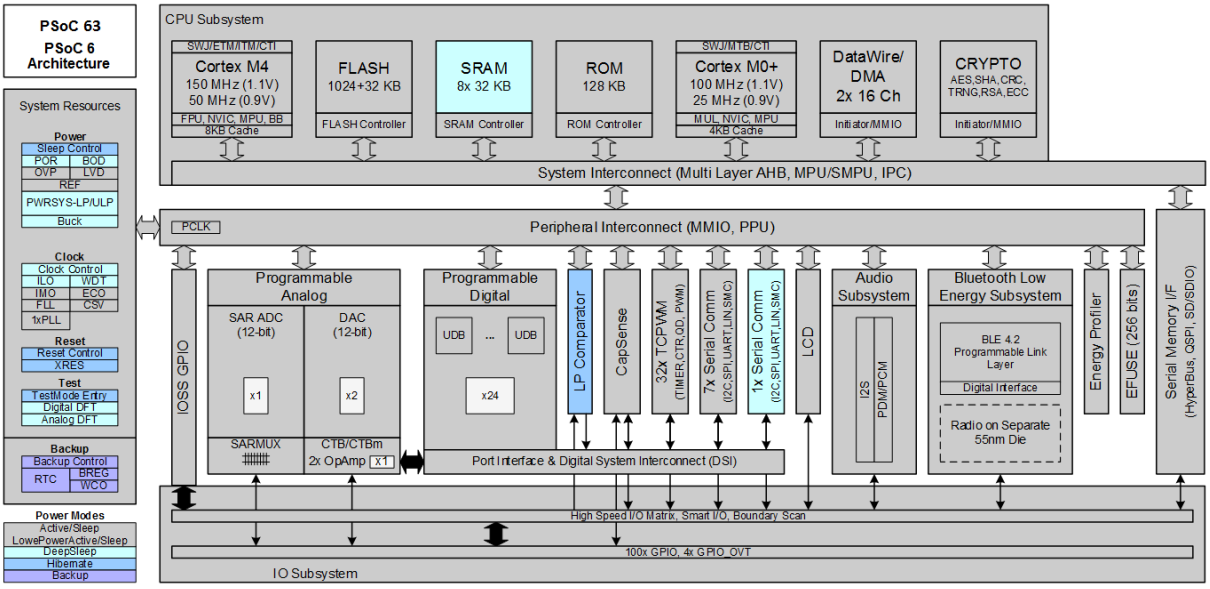


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CYBLE-416045-02
Package Name	43-SMT
Family	PSoC 6
Series	PSoC 63
Max CPU speed (MHz)	150
Flash size (kB)	1024
SRAM size (kB)	288
Vdd range (V)	1.7 to 3.6
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

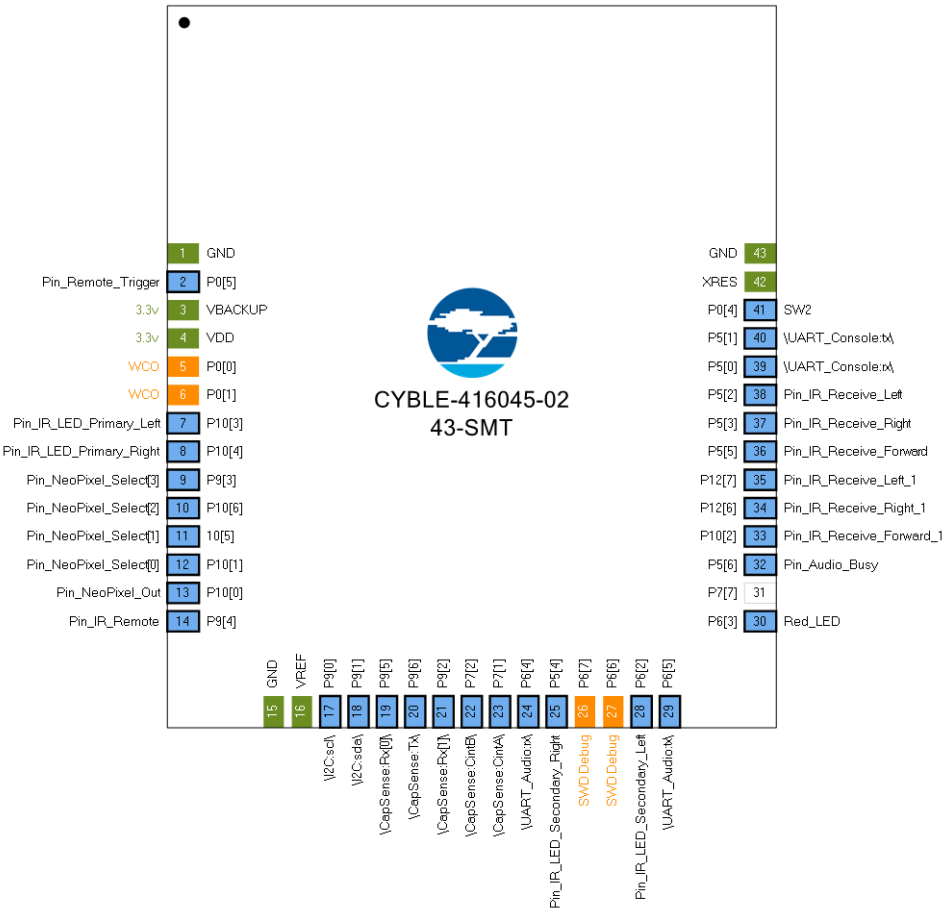
Resource Type	Used	Free	Max	% Used
Digital Clocks	2	6	8	25.00 %
Crypto Accelerator	0	1	1	0.00 %
Interrupts [CM0+]	6	26	32	18.75 %
Interrupts [CM4]	26	121	147	17.69 %
IO	35	1	36	97.22 %
Interprocessor Communication	0	16	16	0.00 %
MCWDT	0	2	2	0.00 %
CapSense	1	0	1	100.00 %
Energy Profiler	0	1	1	0.00 %
Real Time Clock	0	1	1	0.00 %
Bluetooth Low Energy	1	0	1	100.00 %
I2S	0	1	1	0.00 %
PDM/PCM	0	1	1	0.00 %
SCB	4	5	9	44.44 %
DMA Channels	1	31	32	3.13 %
LCD	0	1	1	0.00 %
SmartIO	0	2	2	0.00 %
TCPWM	5	27	32	15.63 %
UDB				
Macrocells	23	73	96	23.96 %
Unique P-terms	19	173	192	9.90 %
Total P-terms	28			
Datapath Cells	0	12	12	0.00 %
Status Cells	1	11	12	8.33 %
Status Registers	1			
Control Cells	2	10	12	16.67 %
Control Registers	2			
7-Bit IDAC	1	1	2	50.00 %
Continuous Time DAC	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
Opamp	0	2	2	0.00 %
Sample and Hold	0	1	1	0.00 %

Resource Type	Used	Free	Max	% Used
SAR ADC	0	1	1	0.00 %
DieTemp Sensor	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
6	GND	GND	Power, Dedicated	
15	P10[6]	Pin_NeoPixel_Select[2]	Software In/Out	Strong drive
16	10[5]	Pin_NeoPixel_Select[1]	Software In/Out	Strong drive
17	P10[1]	Pin_NeoPixel_Select[0]	Software In/Out	Strong drive
18	P10[0]	Pin_NeoPixel_Out	Dgtl Out	Strong drive
19	P9[4]	Pin_IR_Remote	Dgtl In	Res pull up
20	GND	GND	Power, Dedicated	
21	VREF	VREF	Dedicated	
22	P9[0]	\I2C:scl\	Dgtl In	OD, DL
23	P9[1]	\I2C:sda\	Dgtl In	OD, DL
24	P9[5]	\CapSense:Rx[0]\	Analog	HiZ analog
7	P0[5]	Pin_Remote_Trigger	Software In/Out	Res pull up/down
25	P9[6]	\CapSense:Tx\	Analog	HiZ analog
26	P9[2]	\CapSense:Rx[1]\	Analog	HiZ analog
27	P7[2]	\CapSense:CintB\	Analog	HiZ analog
28	P7[1]	\CapSense:CintA\	Analog	HiZ analog
29	P6[4]	\UART_Audio:rx\	Dgtl In	HiZ analog
30	P5[4]	Pin_IR_LED_Secondary_Right	Dgtl Out	Strong drive
31	P6[7]	GPIO [unused]	Dgtl In	Res pull down
32	P6[6]	GPIO [unused]	Dgtl In	Res pull up
33	P6[2]	Pin_IR_LED_Secondary_Left	Dgtl Out	Strong drive
34	P6[5]	\UART_Audio:tx\	Dgtl Out	Strong drive
8	VBACKUP	VBACKUP	Power	
35	P6[3]	Red_LED	Software In/Out	Strong drive
36	P7[7]	GPIO [unused]		
37	P5[6]	Pin_Audio_Busy	Software In/Out	HiZ analog
38	P10[2]	Pin_IR_Receive_Forward_1	Dgtl In	Res pull up
39	P12[6]	Pin_IR_Receive_Right_1	Dgtl In	Res pull up
40	P12[7]	Pin_IR_Receive_Left_1	Dgtl In	Res pull up
41	P5[5]	Pin_IR_Receive_Forward	Dgtl In	Res pull up
42	P5[3]	Pin_IR_Receive_Right	Dgtl In	Res pull up
43	P5[2]	Pin_IR_Receive_Left	Dgtl In	Res pull up
44	P5[0]	\UART_Console:rx\	Dgtl In	HiZ analog
9	VDD	VDD	Power	
45	P5[1]	\UART_Console:tx\	Dgtl Out	Strong drive
46	P0[4]	SW2	Dgtl In	Res pull up
47	XRES	XRES	Dedicated	

Pin	Port	Name	Type	Drive Mode
48	GND	GND	Power, Dedicated	
10	P0[0]	GPIO [unused]	Analog	HiZ analog
11	P0[1]	GPIO [unused]	Analog	HiZ analog
12	P10[3]	Pin_IR_LED_Primary_Left	Dgtl Out	Strong drive
13	P10[4]	Pin_IR_LED_Primary_Right	Dgtl Out	Strong drive
14	P9[3]	Pin_NeoPixel_Select[3]	Software In/Out	Strong drive

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- OD, DL = Open drain, drives low
- HiZ analog = High impedance analog
- Res pull up/down = Resistive pull up/down
- Res pull down = Resistive pull down

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
10[5]	16	Pin_NeoPixel_Select[1]	Software In/Out	Strong drive
P0[0]	10	GPIO [unused]	Analog	HiZ analog
P0[1]	11	GPIO [unused]	Analog	HiZ analog
P0[4]	46	SW2	Dgtl In	Res pull up
P0[5]	7	Pin_Remote_Trigger	Software In/Out	Res pull up/down
P10[0]	18	Pin_NeoPixel_Out	Dgtl Out	Strong drive
P10[1]	17	Pin_NeoPixel_Select[0]	Software In/Out	Strong drive
P10[2]	38	Pin_IR_Receive_Forward_1	Dgtl In	Res pull up
P10[3]	12	Pin_IR_LED_Primary_Left	Dgtl Out	Strong drive
P10[4]	13	Pin_IR_LED_Primary_Right	Dgtl Out	Strong drive
P10[6]	15	Pin_NeoPixel_Select[2]	Software In/Out	Strong drive
P12[6]	39	Pin_IR_Receive_Right_1	Dgtl In	Res pull up
P12[7]	40	Pin_IR_Receive_Left_1	Dgtl In	Res pull up
P5[0]	44	\UART_Console:rx\	Dgtl In	HiZ analog
P5[1]	45	\UART_Console:tx\	Dgtl Out	Strong drive
P5[2]	43	Pin_IR_Receive_Left	Dgtl In	Res pull up
P5[3]	42	Pin_IR_Receive_Right	Dgtl In	Res pull up
P5[4]	30	Pin_IR_LED_Secondary_Right	Dgtl Out	Strong drive
P5[5]	41	Pin_IR_Receive_Forward	Dgtl In	Res pull up
P5[6]	37	Pin_Audio_Busy	Software In/Out	HiZ analog
P6[2]	33	Pin_IR_LED_Secondary_Left	Dgtl Out	Strong drive
P6[3]	35	Red_LED	Software In/Out	Strong drive
P6[4]	29	\UART_Audio:rx\	Dgtl In	HiZ analog
P6[5]	34	\UART_Audio:tx\	Dgtl Out	Strong drive
P6[6]	32	GPIO [unused]	Dgtl In	Res pull up
P6[7]	31	GPIO [unused]	Dgtl In	Res pull down
P7[1]	28	\CapSense:CintA\	Analog	HiZ analog
P7[2]	27	\CapSense:CintB\	Analog	HiZ analog
P7[7]	36	GPIO [unused]		
P9[0]	22	\I2C:scl\	Dgtl In	OD, DL
P9[1]	23	\I2C:sda\	Dgtl In	OD, DL
P9[2]	26	\CapSense:Rx[1]\	Analog	HiZ analog
P9[3]	14	Pin_NeoPixel_Select[3]	Software In/Out	Strong drive
P9[4]	19	Pin_IR_Remote	Dgtl In	Res pull up
P9[5]	24	\CapSense:Rx[0]\	Analog	HiZ analog
P9[6]	25	\CapSense:Tx\	Analog	HiZ analog

Abbreviations used in Table 4 have the following meanings:

- HiZ analog = High impedance analog

- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Res pull up/down = Resistive pull up/down
- Dgtl Out = Digital Output
- Res pull down = Resistive pull down
- OD, DL = Open drain, drives low

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\CapSense:CintA\	P7[1]	Analog
\CapSense:CintB\	P7[2]	Analog
\CapSense:Rx[0]\	P9[5]	Analog
\CapSense:Rx[1]\	P9[2]	Analog
\CapSense:Tx\	P9[6]	Analog
\I2C:scl\	P9[0]	Dgtl In
\I2C:sda\	P9[1]	Dgtl In
\UART_Audio:rx\	P6[4]	Dgtl In
\UART_Audio:tx\	P6[5]	Dgtl Out
\UART_Console:rx\	P5[0]	Dgtl In
\UART_Console:tx\	P5[1]	Dgtl Out
GPIO [unused]	P6[6]	Dgtl In
GPIO [unused]	P0[0]	Analog
GPIO [unused]	P6[7]	Dgtl In
GPIO [unused]	P0[1]	Analog
GPIO [unused]	P7[7]	
Pin_Audio_Busy	P5[6]	Software In/Out
Pin_IR_LED_Primary_Left	P10[3]	Dgtl Out
Pin_IR_LED_Primary_Right	P10[4]	Dgtl Out
Pin_IR_LED_Secondary_Left	P6[2]	Dgtl Out
Pin_IR_LED_Secondary_Right	P5[4]	Dgtl Out
Pin_IR_Receive_Forward	P5[5]	Dgtl In
Pin_IR_Receive_Forward_1	P10[2]	Dgtl In
Pin_IR_Receive_Left	P5[2]	Dgtl In
Pin_IR_Receive_Left_1	P12[7]	Dgtl In
Pin_IR_Receive_Right	P5[3]	Dgtl In
Pin_IR_Receive_Right_1	P12[6]	Dgtl In
Pin_IR_Remote	P9[4]	Dgtl In
Pin_NeoPixel_Out	P10[0]	Dgtl Out
Pin_NeoPixel_Select[0]	P10[1]	Software In/Out
Pin_NeoPixel_Select[1]	10[5]	Software In/Out
Pin_NeoPixel_Select[2]	P10[6]	Software In/Out
Pin_NeoPixel_Select[3]	P9[3]	Software In/Out
Pin_Remote_Trigger	P0[5]	Software In/Out
Red_LED	P6[3]	Software In/Out
SW2	P0[4]	Dgtl In

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Embedded Trace (ETM)	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

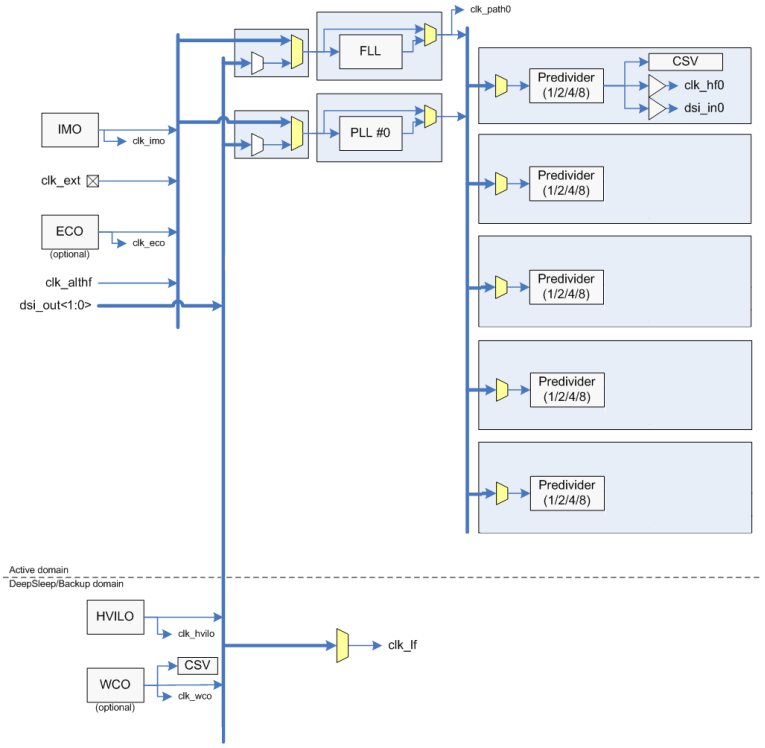
Name	Value
Power Mode	1.1V LDO Linear Regulator
External PMIC Output	Disabled
vBackup Source	VDDD
VBACKUP (V)	3.3
VDD (V)	3.3
Variable VDDA	False

4 Clocks

The clock system includes these clock resources:

- Multiple internal clock sources:
  - 8 MHz Internal Main Oscillator (IMO) ±1%
  - 32 kHz Internal Low Speed Oscillator (ILO) ±30% output
  - 32.768 kHz Precision Internal Low Speed Oscillator (PILO) ±2% output
- Internal FLL and PLL can be used to increase frequency generated by HF clock sources
- Source clocks, FLL, and PLL can be used to drive 5 separate HF clocks
- HFCLK0 can be used to drive peripherals and UDBs
- LFCLK is typically used for DeepSleep wakeup timer

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clk_HF0	NONE	PLL0	150 MHz	150 MHz	±1	True	True
PLL0	NONE	PathMux1	150 MHz	150 MHz	±1	False	True
Clk_Fast	NONE	Clk_HF0	150 MHz	150 MHz	±1	True	True
FLL	NONE	PathMux0	100 MHz	100 MHz	±2.4	True	True
Clk_Slow	NONE	Clk_Peri	75 MHz	75 MHz	±1	True	True
Clk_Peri	NONE	Clk_HF0	75 MHz	75 MHz	±1	True	True
Clk_Pump	NONE	FLL	25 MHz	25 MHz	±2.4	True	True
PathMux4	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_Timer	NONE	IMO	8 MHz	8 MHz	±1	True	True
IMO	NONE		8 MHz	8 MHz	±1	True	True
PathMux1	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux0	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux3	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux2	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_AltSysTick	NONE	Clk_LF	32.768 kHz	32.768 kHz	±0.015	True	True
Clk_Bak	NONE	WCO	32.768 kHz	32.768 kHz	±0.015	True	True
WCO	NONE		32.768 kHz	32.768 kHz	±0.015	False	True
Clk_LF	NONE	WCO	32.768 kHz	32.768 kHz	±0.015	True	True
ILO	NONE		32 kHz	32 kHz	±10	True	True
ExtClk	NONE		24 MHz	? MHz	±0	False	False
PILO	NONE		32.768 kHz	? MHz	±2	False	False
Clk_HF1	NONE	FLL	50 MHz	? MHz	±0.25	False	False
Clk_HF3	NONE	FLL	50 MHz	? MHz	±0.25	False	False
Clk_HF2	NONE	FLL	50 MHz	? MHz	±0.25	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
Clk_HF4	NONE	FLL	50 MHz	? MHz	±0.25	False	False
AltHF	NONE		32 MHz	? MHz	±0	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

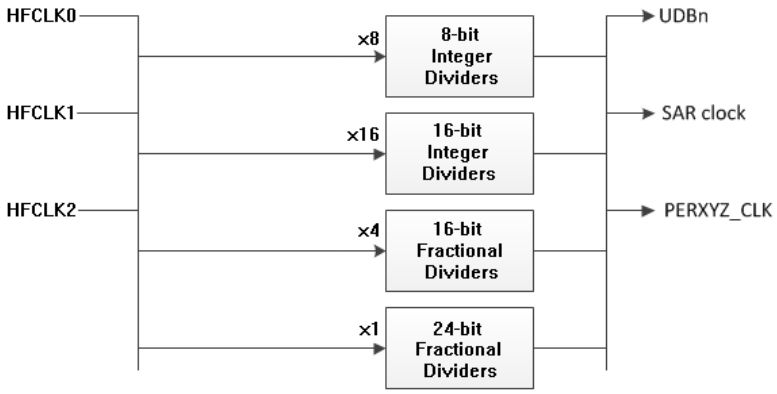


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
SPI_NeoPixel_-SCBCLK	UNKNOWN	Clk_Peri	12.5 MHz	12.5 MHz	±1	True	True
Clock_FC	UNKNOWN	Clk_Peri	12 MHz	12.5 MHz	±1	True	True
I2C_SCBCLK	UNKNOWN	Clk_Peri	1.55 MHz	1.562 MHz	±1	True	True
UART_-Console_-SCBCLK	UNKNOWN	Clk_Peri	1.382 MHz	1.389 MHz	±1	True	True
Bit_Stream_-Timer_Clock	UNKNOWN	Clk_Peri	1 MHz	1 MHz	±1	True	True
Tag_Sensor_-Bit_Stream_-Timer_Clock	UNKNOWN	Clk_Peri	1 MHz	1 MHz	±1	True	True
CapSense_-ModClk	UNKNOWN	Clk_Peri	? MHz	294.118 kHz	±1	True	True
UART_Audio_-SCBCLK	UNKNOWN	Clk_Peri	115.2 kHz	115.207 kHz	±1	True	True
SW_CLK	UNKNOWN	Clk_Peri	50 Hz	50 Hz	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 6 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	CortexM0p Vector	CortexM0p Priority	CortexM4 Vector	CortexM4 Priority	Deep Sleep Wakeup Capable
SW2_Int	15			15	7	CortexM4
BLE_bless_isr	24	3	3			CortexM0p
SPI_-NeoPixel_-SCB_IRQ	42			42	7	No
I2C_SCB_IRQ	43			43	7	No
Int_UART_-Console	46			46	7	No
UART_-Audio_-SCB_IRQ	47			47	7	No
CapSense_ISR	49			49	7	No
DMA_-NeoPixel_-Int	50			50	7	No
Remote_-Tag_-Sensor_-Bit_-Stream_-Timer_-Interrupt	90			90	7	No
Local_Tag_-Sensor_-Bit_-Stream_-Timer_-Interrupt_1	91			91	7	No
Local_Tag_-Sensor_-Bit_-Stream_-Timer_-Interrupt	92			92	7	No
Bit_-Stream_-Timer_-Interrupt	94			94	7	No
Forward_-Tag_-Sensor_-Falling_-Edge_ISR	122			122	7	No

Name	Intr Num	CortexM0p Vector	CortexM0p Priority	CortexM4 Vector	CortexM4 Priority	Deep Sleep Wakeup Capable
Forward_-Tag_-Sensor_-Falling_-Edge_ISR_-1	123			123	7	No
Forward_-Tag_-Sensor_-Rising_-Edge_ISR	124			124	7	No
Forward_-Tag_-Sensor_-Rising_-Edge_ISR_-1	125			125	7	No
Left_Tag_-Sensor_-Falling_-Edge_ISR	126			126	7	No
Left_Tag_-Sensor_-Falling_-Edge_ISR_-1	127			127	7	No
Left_Tag_-Sensor_-Rising_-Edge_ISR	128			128	7	No
Left_Tag_-Sensor_-Rising_-Edge_ISR_-1	129			129	7	No
Remote_-Tag_-Sensor_-Falling_-Edge_ISR	130			130	7	No
Remote_-Tag_-Sensor_-Rising_-Edge_ISR	131			131	7	No
Right_Tag_-Sensor_-Falling_-Edge_ISR	132			132	7	No
Right_Tag_-Sensor_-Falling_-Edge_ISR_-1	133			133	7	No

Name	Intr Num	CortexM0p Vector	CortexM0p Priority	CortexM4 Vector	CortexM4 Priority	Deep Sleep Wakeup Capable
Right_Tag_-Sensor_-Rising_-Edge_ISR	134			134	7	No
Right_Tag_-Sensor_-Rising_-Edge_ISR_-1	135			135	7	No
Trigger_-Interrupt	136			136	7	No

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 6 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 12. DMAs

Name	Priority	Channel Number
DMA_NeoPixel	3	0

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 6 Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 6 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

This design has no flash protection specified; all blocks are unprotected.

For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the PSoC 6 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

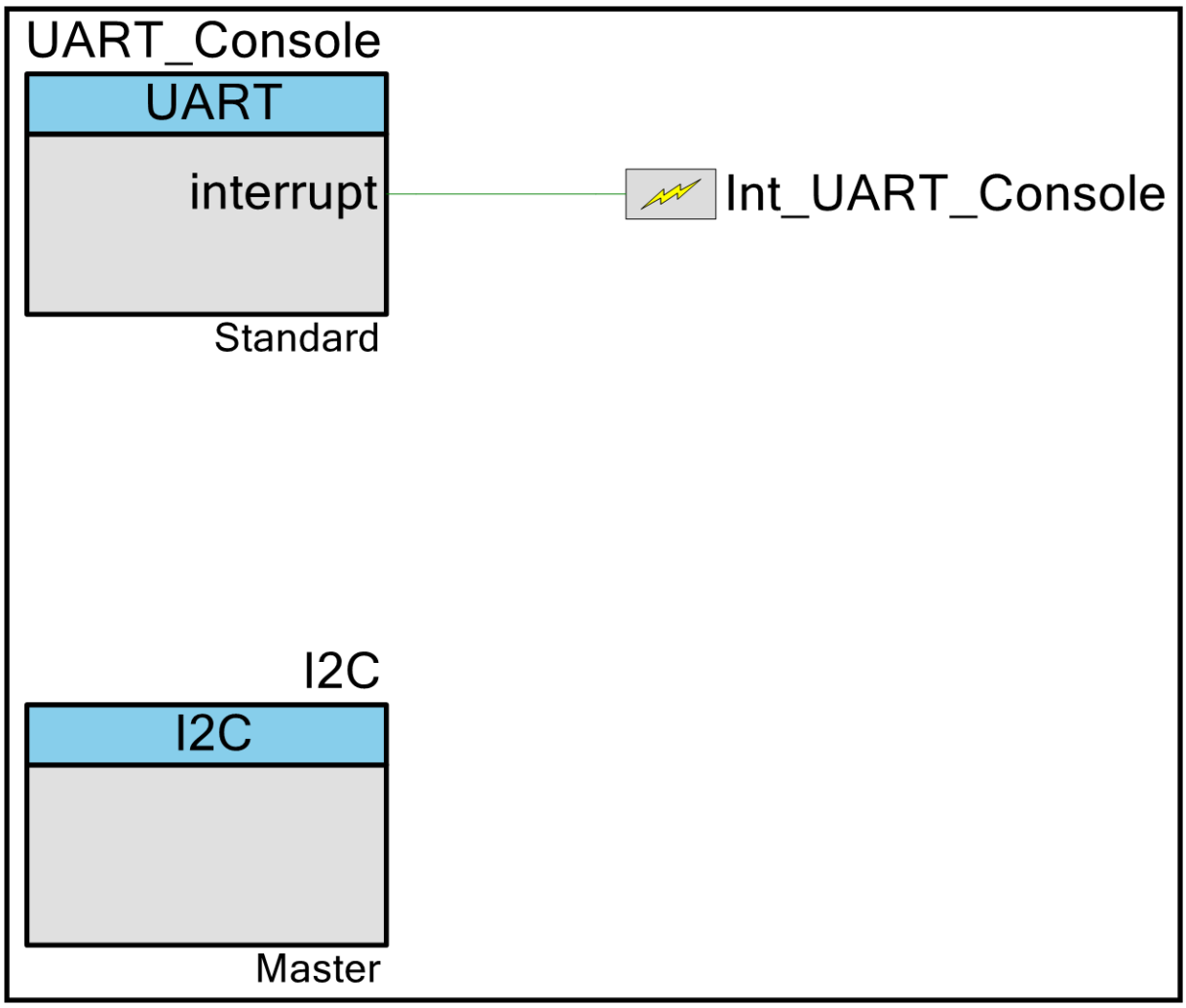
This design's schematic content consists of the following 11 schematic sheets:

7.1 Schematic Sheet: Title

Figure 5. Schematic Sheet: Title

7.2 Schematic Sheet: Communications

Figure 6. Schematic Sheet: Communications

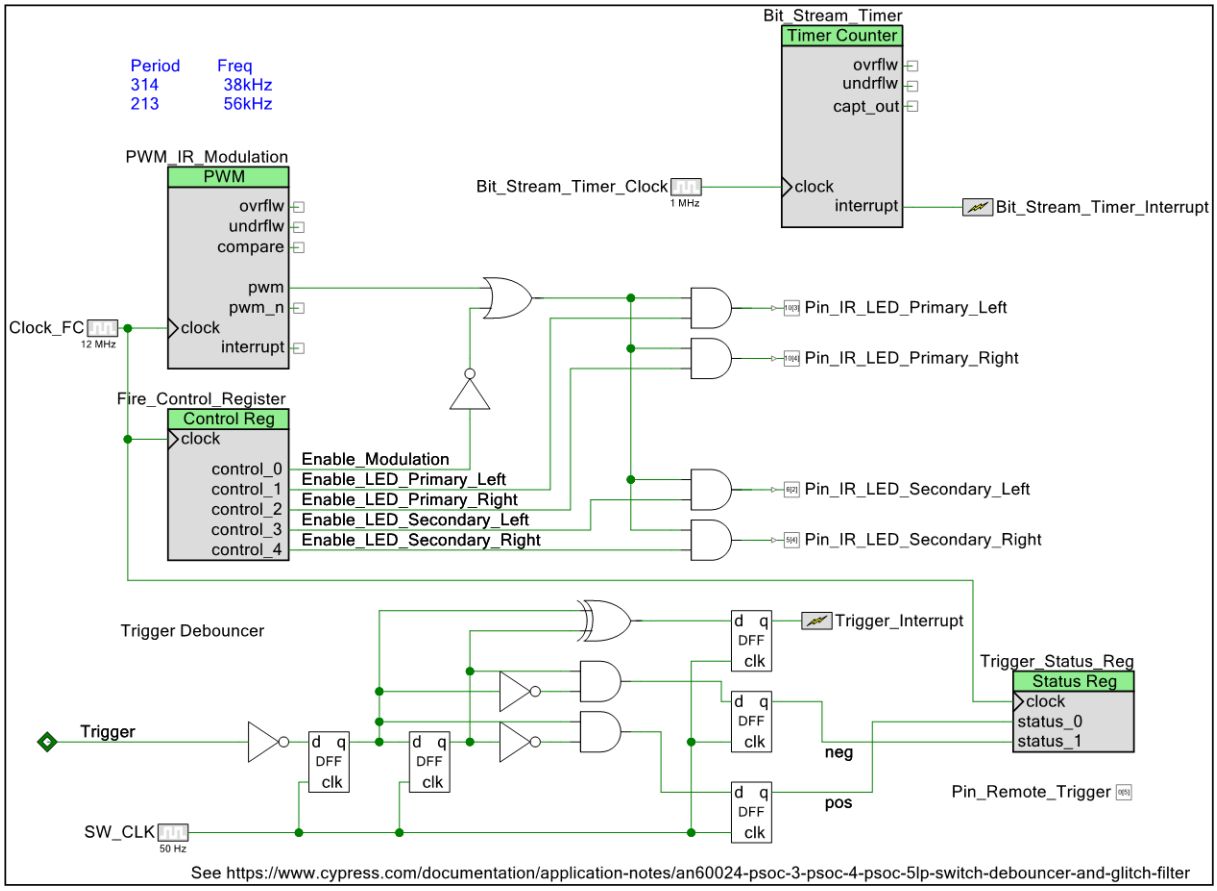


This schematic sheet contains the following component instances:

- Instance I2C (type: SCB_I2C_PDL_v2_0)
- Instance UART_Console (type: SCB_UART_PDL_v2_0)

7.3 Schematic Sheet: Fire Control

Figure 7. Schematic Sheet: Fire Control

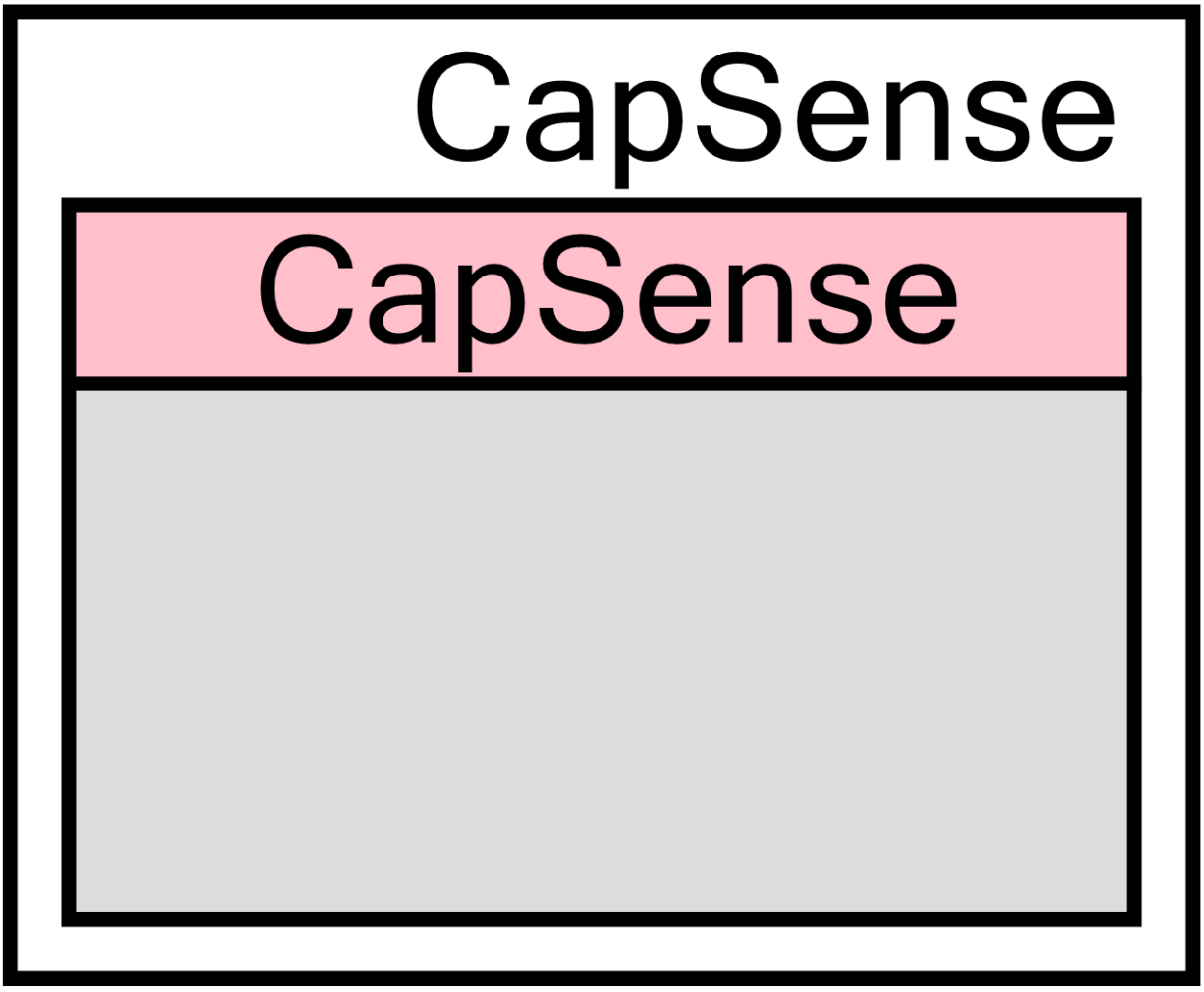


This schematic sheet contains the following component instances:

- Instance Bit_Stream_Timer (type: TCPWM_Counter_PDL_v1_0)
- Instance cydff_1 (type: cydff_v1_30)
- Instance cydff_2 (type: cydff_v1_30)
- Instance cydff_3 (type: cydff_v1_30)
- Instance cydff_4 (type: cydff_v1_30)
- Instance cydff_5 (type: cydff_v1_30)
- Instance Fire_Control_Register (type: CyControlReg_v1_80)
- Instance PWM_IR_Modulation (type: TCPWM_PWM_PDL_v1_0)
- Instance Trigger_Status_Reg (type: CyStatusReg_v1_90)

7.4 Schematic Sheet: CapSense

Figure 8. Schematic Sheet: CapSense

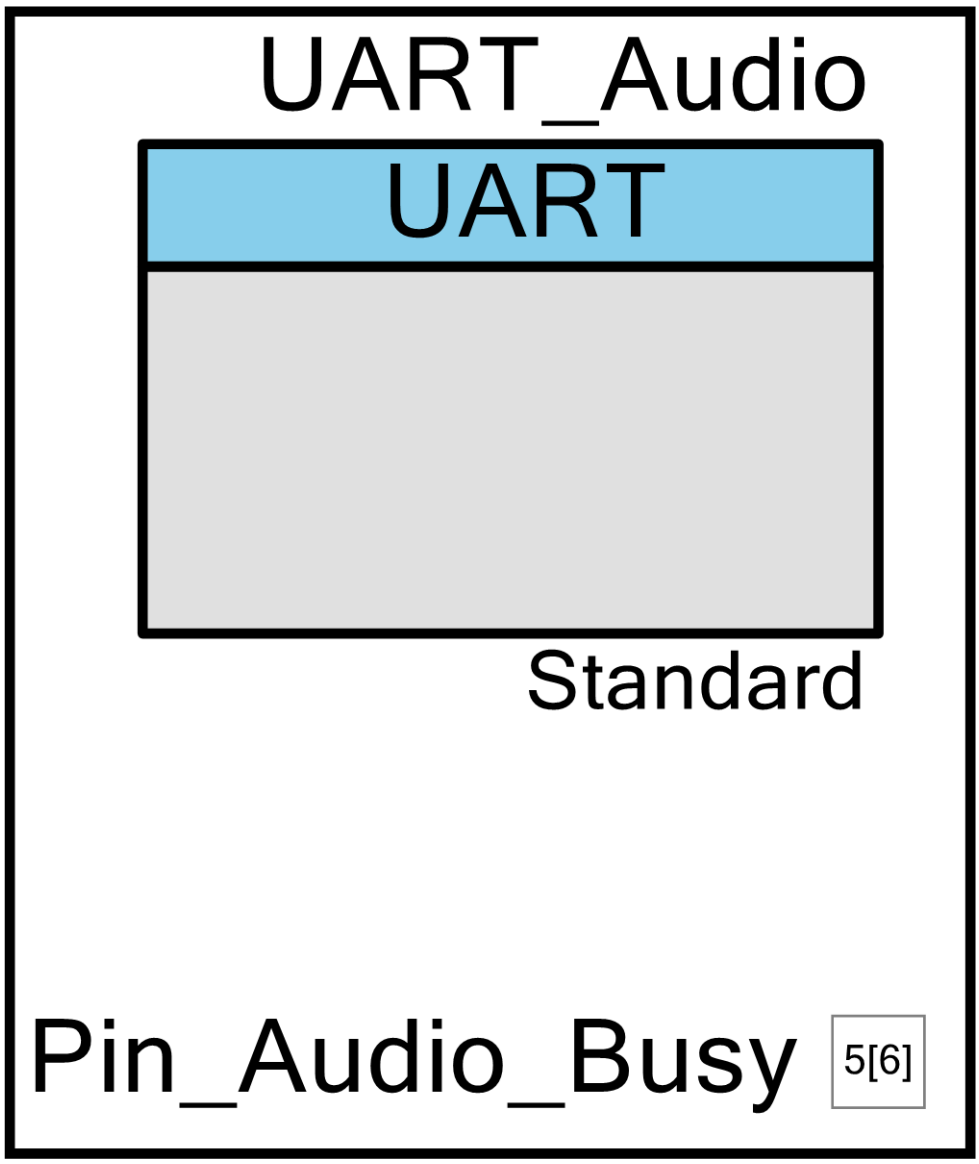


This schematic sheet contains the following component instances:

- Instance CapSense (type: CapSense_v3_0)

7.5 Schematic Sheet: Audio

Figure 9. Schematic Sheet: Audio

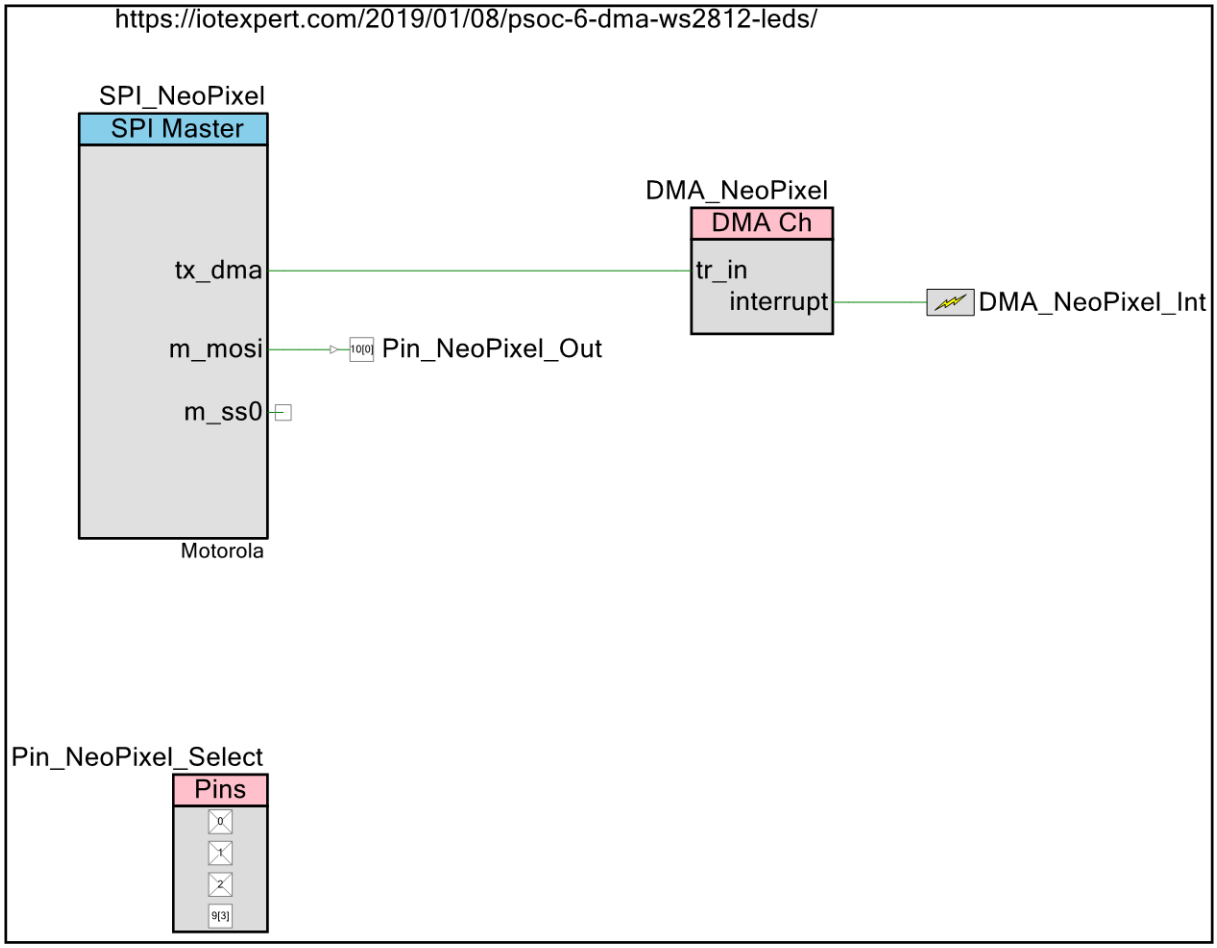


This schematic sheet contains the following component instances:

- Instance UART_Audio (type: SCB_UART_PDL_v2_0)

7.6 Schematic Sheet: Displays

Figure 10. Schematic Sheet: Displays

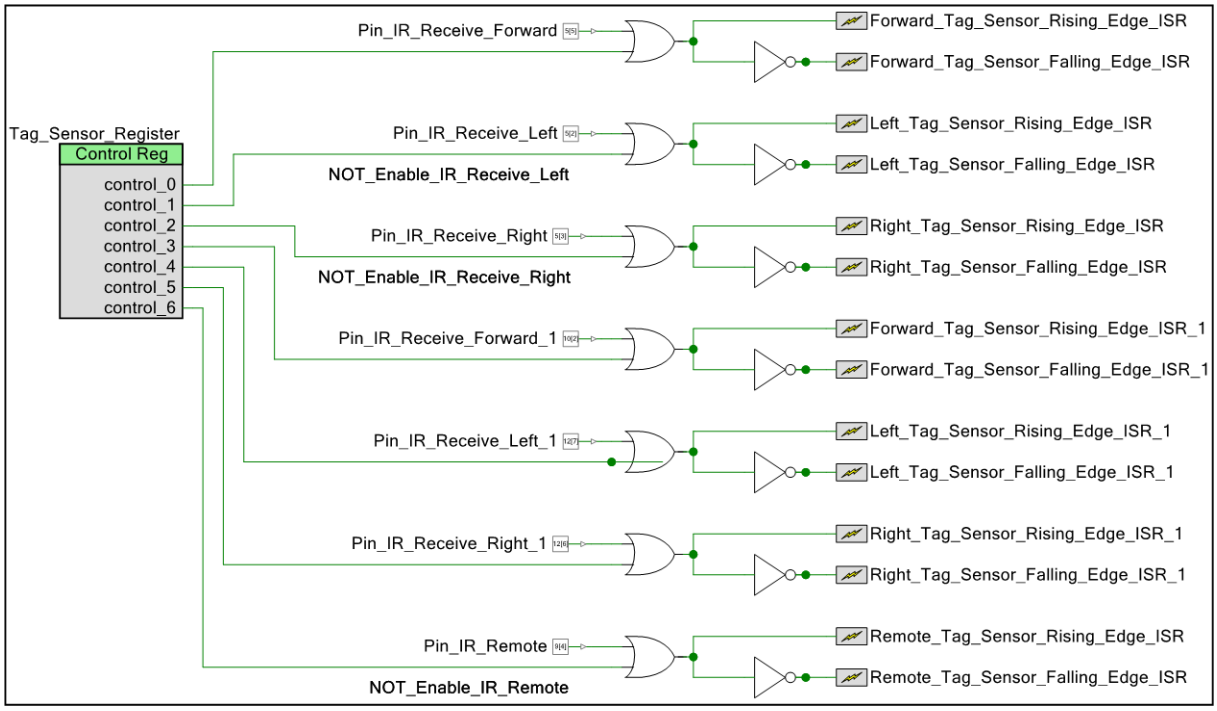


This schematic sheet contains the following component instances:

- Instance SPI_NeoPixel (type: SCB_SPI_PDL_v2_0)

7.7 Schematic Sheet: Tag Sensors

Figure 11. Schematic Sheet: Tag Sensors

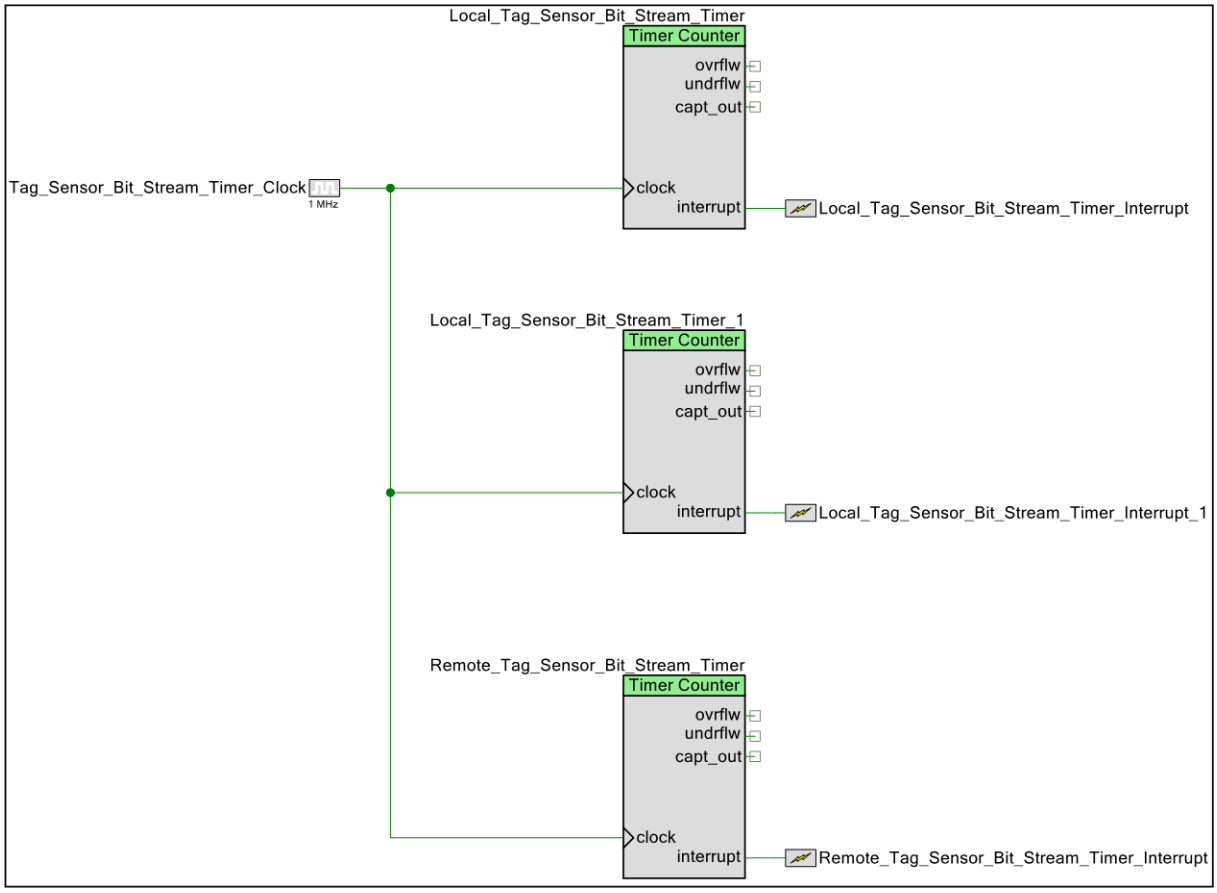


This schematic sheet contains the following component instances:

- Instance Tag_Sensor_Register (type: CyControlReg_v1_80)

7.8 Schematic Sheet: Tag Sensor Timers

Figure 12. Schematic Sheet: Tag Sensor Timers

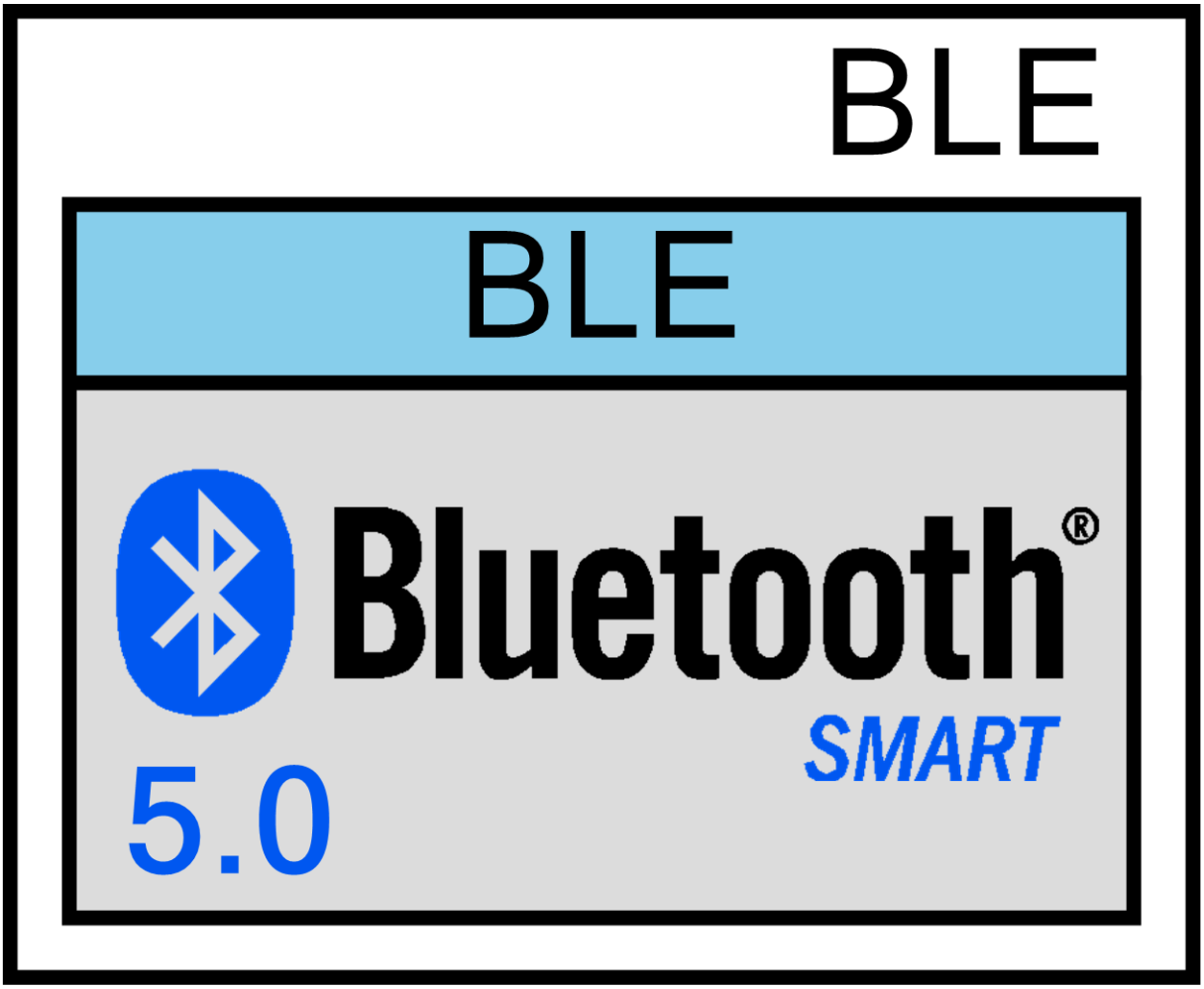


This schematic sheet contains the following component instances:

- Instance Local_Tag_Sensor_Bit_Stream_Timer (type: TCPWM_Counter_PDL_v1_0)
- Instance Local_Tag_Sensor_Bit_Stream_Timer_1 (type: TCPWM_Counter_PDL_v1_0)
- Instance Remote_Tag_Sensor_Bit_Stream_Timer (type: TCPWM_Counter_PDL_v1_0)

7.9 Schematic Sheet: BLE

Figure 13. Schematic Sheet: BLE

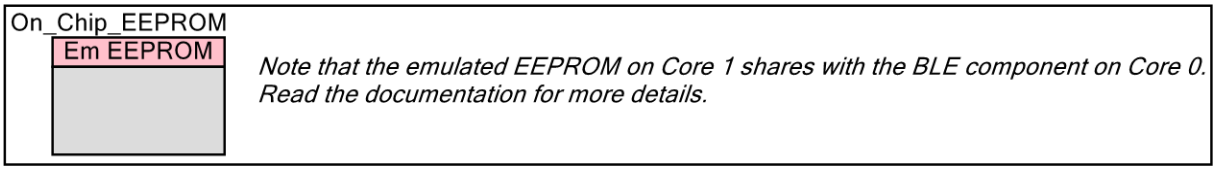


This schematic sheet contains the following component instances:

- Instance BLE (type: BLE_PDL_v2_20)

7.10 Schematic Sheet: EEPROM

Figure 14. Schematic Sheet: EEPROM

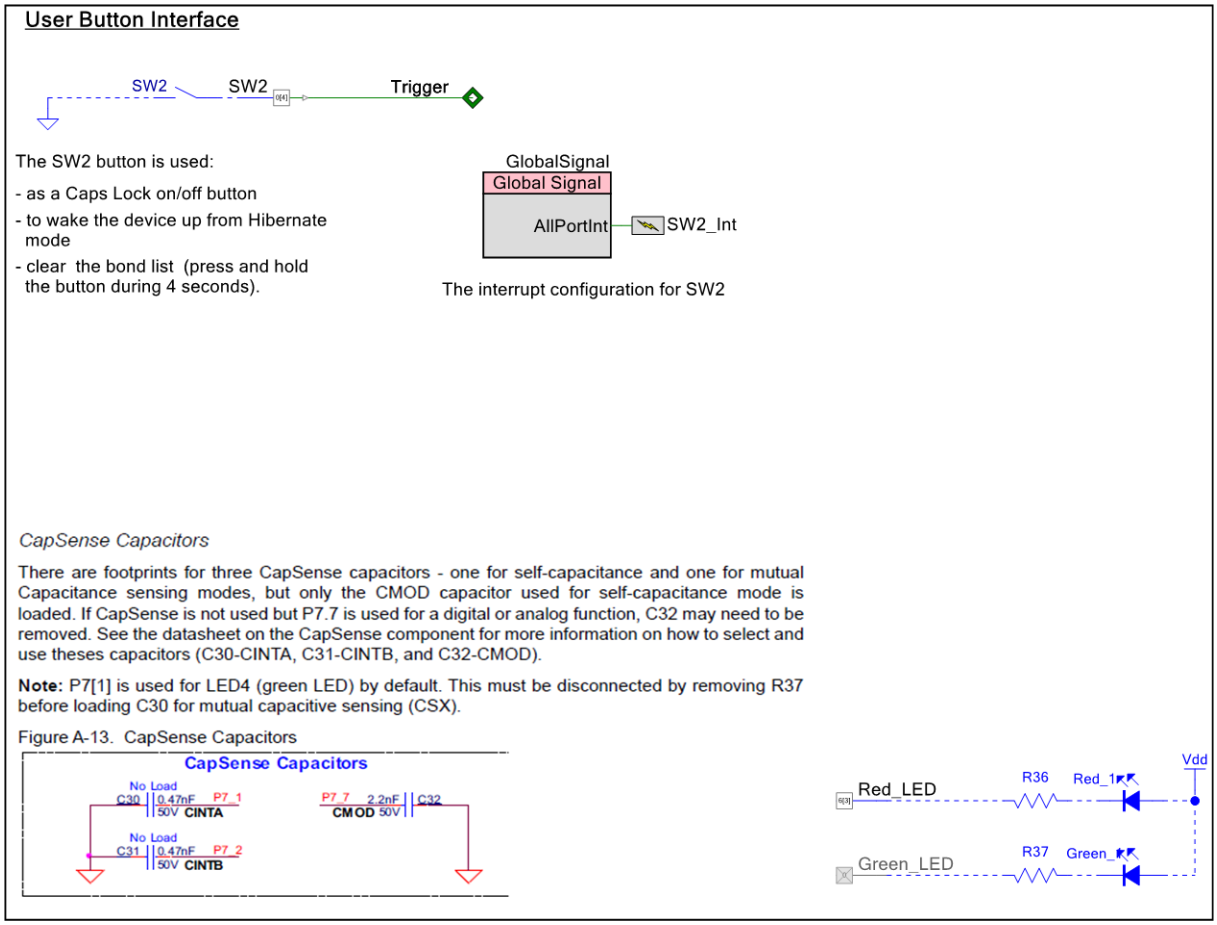


This schematic sheet contains the following component instances:

- Instance On_Chip_EEPROM (type: Em_EEPROM_v2_20)

7.11 Schematic Sheet: CY8CPROTO-063-BLE Built-In

Figure 15. Schematic Sheet: CY8CPROTO-063-BLE Built-In



8 Components

8.1 Component type: BLE_PDL [v2.20]

8.1.1 Instance BLE

Description: Bluetooth Low Energy (BLE)
Instance type: BLE_PDL [v2.20]
Datasheet: online component datasheet for BLE_PDL

Table 13. Component Parameters for BLE

Parameter Name	Value	Description
AddQdepthPerConn	0	Additional stack queue depth per connection for better throughput. Default queue is defined by CYBLE_L2CAP_-STACK_Q_DEPTH_PER_-CONN macro.
AutopopulateWhitelist	true	Provides an option to link the whitelist to the bonded device list.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
ConnectionCount	4	The number of BLE connections / links.
Enable LE 2 Mbps	false	Enable LE 2 Mbps feature.
Enable Link Layer Privacy	false	Enables LL Privacy 1.2 feature of Bluetooth 4.2.
EnableExternalLnaRxOutput	false	When selected, ext_lna_rx_ctl_-out signal from the BLE radio is routed on a GPIO.
EnableExternalPaLnaOutput	false	Enables external PA and LNA chip enable control pins and automatically enables routing the BLESS Tx and Rx enable signals on the dedicated GPIO lines.
EnableExternalPaTxOutput	false	When selected, ext_pa_tx_ctl_-out signal from the BLE radio is routed on a GPIO.
EnableExternalPrepWriteBuff	false	Enables application to provide dynamically allocated buffer for prepare write request. The buffer should be allocated and provided after CYBLE_EVT_-MEMORY_REQUEST event from stack.
EnableL2capLogicalChannels	true	Enables L2CAP logical channels support.
HalBaudRate	115200	UART baud rate
HalCtsEnable	true	In the HCI mode, the parameter enables the cts output in the UART.

Parameter Name	Value	Description
HalCtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output cts signal of the UART.
HalOversampling	13	UART oversampling
HalRtsEnable	true	In the HCI mode, the parameter enables the rts output in the UART.
HalRtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output rts signal of the UART.
HalRtsTriggerLevel	120	In the HCI mode, the parameter specifies the number of entries in the RX FIFO to activate the rts output signal of the UART.
HciContrCore	CortexM0p	Defines the core for the Controler in HCI mode.
HostCore	CortexM4	Defines the core for the Host. For DUAL core device Controller will be compiled for different core.
ImportFilePath		The path to the file shared by another BLE component instance.
KeypressNotifications	false	Provides an option for a keyboard-only device during the LE secure pairing process to send key press notifications when the user enters or deletes a key.
L2capMpsSize	23	The maximum size of payload data that the L2CAP layer is capable of accepting.
L2capMtuSize	23	The maximum SDU size of an L2CAP packet.
L2capNumChannels	1	The number of LE L2CAP connection oriented logical channels required by the application.
L2capNumPsm	1	The number of PSMs required by the application.
Link layer max RX payload size (bytes)	27	The maximum link layer receive payload size to be used in the design.
Link layer max TX payload size (bytes)	27	The maximum link layer transmit payload size to be used in the design.
MaxBondedDevices	16	The maximum number of bonded devices to be supported by this device.
MaxResolvableDevices	16	The maximum number of peer devices whose addresses should be resolved by this device.
MaxWhitelistSize	16	The maximum number of devices that can be added to the whitelist.

Parameter Name	Value	Description
Mode	Profile	Defines the component operating mode.
Radio Power Calibration	false	Enables TX Power Calibration Retention
SharingMode	None	Defines if some parts of code are shared between two BLE components.
StackMode	Dual IPC	Determines the internal stack mode. Is used to switch the operation for debugging. Release - Host and Controller on single core with software interface DualIPC - Host and Controller on dual core with IPC interface HostOnly - Host with UART interface HostOnlyIPC - Host with IPC interface DualUart - Host and Controller on dual core with UART interface
StrictPairing	false	Provides an option to use only the selected security features and doesn't fallback to an unsecure connection if the peer device doesn't support the selected security features.
UseDeepSleep	true	Indicates whether deep sleep mode is used.
User Comments		Instance-specific comments.

8.2 Component type: CapSense [v3.0]

8.2.1 Instance CapSense

Description: (custom component)
Instance type: CapSense [v3.0]
Datasheet: online component datasheet for CapSense

Table 14. Component Parameters for CapSense

Parameter Name	Value	Description
AdcTotalChannels	0	The total input channels to ADC. The range of valid value is from 1 (ADC_CSD component) or 0 (CapSense_ADC component) t 10. The ADC functionality of CapSense_ADC component is disabled when a parameter value is set to 0.
Ballistic Enable	false	Enables the Ballistic filter for th component.

Parameter Name	Value	Description
BaselineType	IIR	Selects the type of baseline needed for design. IIR (default) - Selects the IIR filter based baseline algorithm CY (Bucket) Baseline - Selects Cypress' "bucket" method for the baseline algorithm.
BlockOffAfterScanEnable	false	Enable the turning-off block after a scan to save additiona power. Disabled (default) - The CSD block will be always turned ON This allows the other components (IDAC) work alon with CapSense component in project. Enabled - The CSD block will b turned ON only during a scan
Centroid4PtsEnable	false	Enables the 4-point method of maxima finding for single dimension sliders.
Config Data in Flash	true	Controls whether the configuration structure is store in flash (const, true) or SRAM (not const, false).
CsdEnable	false	The internal parameter automatically enabled by the customizer when at least one widget uses the CSD sensing mode AND the dual-channel CSD (CSD2x) is not selected.
CsdMFSDividerOffsetF1	1	
CsdMFSDividerOffsetF2	2	
CsdSensingMethod	Legacy	
CsdV2AnalogWakeupDelayUs	0	Defines delay in the CapSense_Wakeup() API tha is intended to ensure proper initialization of the CSDV2 analog part.
Csx0IdacGainV2	Medium (300 nA/bit)	Selects the IDAC gain setting for CSX sensing on CSD bloc 0. Applicable only for CSDv2 IP.
CsxAnalogStartupDelayUs	23	Defines delay prior to start of the scan, that is intended to ensure proper initialization of the CSDV2 analog part.
CsxAutoZeroEnable	false	Enables auto-zero prior to fine initialization for the CSX sensin method.
CsxCommonTxClockEnable	true	When selected, all CSX widget share the same Tx clock with the frequency specified in the Tx clock frequency (kHz) parameter. Otherwise, a Tx clock frequenc can be entered separately for each CSX widget in the Widget Details tab.

Parameter Name	Value	Description
CsxEnable	true	The internal parameter automatically enabled by the customizer when at least one widget uses the CSX sensing mode AND dual-channel CSX (CSX2x) is not selected.
CsxFineInitCycles	4	Sets a fine-init time period
CsxIdacAutoCalibrateEnable	true	When enabled, IDACs values for the CSX widgets are automatically set by the component. It is recommended to select Enable IDAC auto-calibration fo robust operation.
CsxIdacBitsUsedV2	7	Controls how many of the IDAC bits should be considered for auto-calibration of the CSX widgets. Less bits leads to faster calibration time. Applicable only for CSDv2 IP.
CsxInitShieldSwitchRes	High	Selects the resistance of switches used to drive the shield electrode when an internal shield drive is used.
CsxInitSwitchRes	Medium	Selects the resistance of switches used for Cint1 and Cint2 initialization.
CsxMaxFingers	1	Indicates the maximum numbe of reported fingers. If the number of fingers on the touchpad exceeds this numbe no finger will be reported.
CsxMaxLocalPeaks	5	The maximum possible numbe of local maxima for CSX touchpad.
CsxMFSDividerOffsetF1	1	
CsxMFSDividerOffsetF2	2	
CsxModClockFreq	50000	Selects the modulator clock frequency used for the CSX sensing method. Enter any value between the min and max limits based on th availability of the clock divider
CsxMultiphaseTxEnable	false	Enable/disable the multi-phase scan for CSX.
CsxNoiseMetricEnable	false	Enables the noise metric evaluation for the CSX scan.
CsxPinAliasRx	Button0_Rx0, Button0_Rx1	Contains a comma-separated list of the Rx electrode aliases for the CSX widgets. Used by the Rx pin on the component schematic. Applicable only if CSX2x is disabled.

Parameter Name	Value	Description
CsxPinAliasTx	Button0_Tx	Contains a comma-separated list of the Tx electrode aliases for the CSX widgets. Used by the Tx/Tx2x pins on th component schematic.
CsxPinCountRx	2	Contains the total count of the Rx electrodes for the CSX widgets. Used by the Rx pin on the component schematic. Applicable only if CSX2x is disabled.
CsxPinCountTx	1	Contains the total count of the Rx electrodes for the CSX widgets. Used by the Tx/Tx2x pin on th component schematic.
CsxRawCountCalibrationLevel	40	Represents the rawcount calibration level (percentage) t be used when auto-calibration of the CSX widgets is enabled
CsxScanShieldSwitchRes	Low	Selects the resistance of switches used to drive the shield electrode when an internal shield drive is used.
CsxScanSwitchRes	Low	Selects the resistance of switches used for Cint1 and Cint2 initialization.
CsxSkipAndOversampleNodes	false	Enable/Disable over sampling and scan skip on specific nodes.
CsxTxClockFreq	300	Sets the CSX Tx clock frequency. The highest Tx clock frequenc producing the maximum signa and is the recommended setting. When the Enable common Tx clock is unselected, a Tx Clock frequency can be set individually for each widget in the Widget Details tab.
CsxTxClockSource	Auto	A Tx clock is used to sample th input sensor. The Spread Spectrum Clock (SSC) provides a dithering cloc source with the center frequency equal to the frequency set in the Tx Clock frequency parameter. Direct source disables the SSC source and uses a fixed-frequency clock. Auto is the recommended cloc source selection.

Parameter Name	Value	Description
CustomDataStructSize	0	0 - indicates no custom parameters are added to "CapSense_dsRam" data structure. Non-zero value adds uint8 arra (with size specified by value o this parameter) to global parameters of "CapSense_- dsRam" data structure.
Gesture Enable	false	Defines if the gestures are enabled on the Gestures tab.
Gesture Global Enable	false	Enables the Gesture library fo the component.
IrefSel	SRSS	Select Iref supply.
LowBaselineResetSize	8 bits	Represents a low baseline rese size for sensors.
LpModeEn	false	Select the power mode for the CSD components (REFGEN, AMBUF, CSDCMP, HSCMP): false: High Power mode true: Low Power mode
MultiFreqScanEnable	false	Indicates whether multi-frequency scanning is enabled
NumCentroids	1 (Legacy)	Selects a number of centroid supported on sliders. The available options are 1, 2 or 3 The default is 1 (Legacy). Applicable only to Radial and Linear slider widgets. Not supported on diplexed sliders
OffDebounceEnable	false	Indicates whether the debounc for ON to OFF transition is enabled.
PosIirFilterCoeff	128	The centroid Position IIR filter coefficient for sliders and touchpads. The range of valid values is 1-255.
ProxAverageFilterEnable	false	The finite impulse response filter (no feedback) with equall weighted coefficients. It takes four of most recent samples and computes their average. Eliminates the periodic noise (e.g. noise from AC remains). Applicable only to proximity widgets.
ProxCustomFilterEnable	false	Enables the custom filter. Applicable only to proximity widgets.
ProxIirFilterBaselineN	1	Baseline IIR filter coefficient selection for sensors in proximity widgets. The range of valid values is 1- 255.
ProxIirFilterBaselineType	Performance	Applicable only to proximity widgets.

Parameter Name	Value	Description
ProxIirFilterEnable	false	Enables the infinite-impulse response filter with a step response similar to an RC low pass filter thereby passing the low frequency signals (finger touch responses). Applicable only to proximity widgets.
ProxMedianFilterEnable	false	Enables a non-linear filter that takes three of most recent samples and computes the median value. This filter eliminates spikes noise typically caused by motors and switching power supplies. Applicable only to proximity widgets.
RadialSliderPosIirResetThr	35	Configures reset threshold of position IIR filter for Radial slider widget. When difference between between input positio and filter history is bigger than the threshold then the filter history is reset with input position. Valid range [25..50] i terms of maximum position percentage.
RegularAverageFilterEnable	false	The finite-impulse response filter (no feedback) with equall weighted coefficients. It takes four of most recent samples and computes their average. Eliminates the periodic noise (e.g. noise from AC remains). Applicable only to regular (non proximity) widgets.
RegularCustomFilterEnable	false	Enables the custom filter. Applicable only to regular (non proximity) widgets.
RegularIirFilterBaselineN	1	Baseline IIR filter coefficient selection for sensors in non-proximity widgets. The range of valid values is 1-255.
RegularIirFilterBaselineType	Performance	
RegularIirFilterEnable	false	Enables the infinite-impulse response filter with a step response similar to an RC low pass filter thereby passing low frequency signals (finger touch responses). Applicable only to regular (non proximity) widgets.

Parameter Name	Value	Description
RegularMedianFilterEnable	false	Enables a non-linear filter that takes three of most recent samples and computes the median value. This filter eliminates spikes noise typically caused by motors and switching power supplies. Applicable only to regular (non proximity) widgets.
SecondFinger5x5FilterEnable	false	Enables position filtering of the second touch. Applicable only t CSD touchpad widgets with 5x centroid and two finger detection enabled.
SelfTestEnable	false	The BIST/Class-B library supports the following: the sensor short test, test baseline and raw count limits, CRC for widget-specific register map data, measuring an external ca (Cmod, Csh_tank, CintA and CintB) value and test baseline data consistency. Additionally, measuring of VDDA and two internal reference caps are supported for CSDv2.
SensorAutoResetEnable	false	When enabled, the baseline is always updated and when disabled, the baseline is updated only when the difference between the baselin and raw count is less than the noise threshold. The sensor auto-reset prevent the sensor from permanently turning on when the raw coun accidentally rises because of a large power-supply voltage fluctuation or due to other spurious conditions.
SliderMultiplierMethod	MaxPos / (SnsNum -1)	Defines the method of multiplie calculation for linear slider widget
ThresholdSize	16 bits	Selects a data size for widgets in the component. This applies to Finger Threshol (all widgets) and Proximity Touch Threshold (proximity widgets). In SmartSense (Full Auto-tune mode, parameter value is ignored and threshold register size is always 16-bit.
Timestamp Interval	1	Defines the increment value fo the timestamp register.
TouchpadDisplaySettings		

Parameter Name	Value	Description
TouchpadMultiplierMethod	MaxPos / (SnsNum -1)	Defines the method of multiplie calculation for touchpad widge (is not applicable for CSD 5x5 touchpad)
TouchProxThresholdCoeff	300	Sets coefficient to define touch threshold for proximity sensors
TunerLayoutPreferences		
TunerOptionsPreferences		
TunerViewPreferences		
TunerWidgetData		
Two-finger Settling time (ms)	3	This parameter defines a dela threshold that must be met before two finger gestures are computed. This parameter help to avoid instances where a two finger gesture is reported when two fingers are placed on the panel one after the other.
User Comments		Instance-specific comments.
VrefSel	SRSS	Select Vref supply.
WidgetBaselineCoeffEnable	false	Enables setting of baseline coefficient separately for each widget.

8.3 Component type: CyControlReg [v1.80]

8.3.1 Instance Fire_Control_Register

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 15. Component Parameters for Fire_Control_Register

Parameter Name	Value	Description
Bit0Mode	SyncMode	Defines bit 0 mode
Bit1Mode	SyncMode	Defines bit 1 mode
Bit2Mode	SyncMode	Defines bit 2 mode
Bit3Mode	SyncMode	Defines bit 3 mode
Bit4Mode	SyncMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
ExternalReset	false	Shows the reset terminal
NumOutputs	5	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.3.2 Instance Tag_Sensor_Register

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 16. Component Parameters for Tag_Sensor_Register

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
ExternalReset	false	Shows the reset terminal
NumOutputs	7	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.4 Component type: cydff [v1.30]

8.4.1 Instance cydff_1

Description: D Flip Flop with configurable reset and preset
Instance type: cydff [v1.30]
Datasheet: online component datasheet for cydff

Table 17. Component Parameters for cydff_1

Parameter Name	Value	Description
ArrayWidth	1	Width of d and q terminals. Must be between 1 and 32.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
MultiPresetReset	true	Defines options to set the preset and reset to be either a bus or a single bit.
PresetOrReset	None	Preset/ Reset parameter
SmallMode	true	
User Comments		Instance-specific comments.

8.4.2 Instance cydff_2

Description: D Flip Flop with configurable reset and preset
Instance type: cydff [v1.30]
Datasheet: online component datasheet for cydff

Table 18. Component Parameters for cydff_2

Parameter Name	Value	Description
ArrayWidth	1	Width of d and q terminals. Must be between 1 and 32.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
MultiPresetReset	true	Defines options to set the preset and reset to be either a bus or a single bit.
PresetOrReset	None	Preset/ Reset parameter
SmallMode	true	
User Comments		Instance-specific comments.

8.4.3 Instance cydff_3

Description: D Flip Flop with configurable reset and preset
Instance type: cydff [v1.30]
Datasheet: online component datasheet for cydff

Table 19. Component Parameters for cydff_3

Parameter Name	Value	Description
ArrayWidth	1	Width of d and q terminals. Must be between 1 and 32.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
MultiPresetReset	true	Defines options to set the preset and reset to be either a bus or a single bit.
PresetOrReset	None	Preset/ Reset parameter
SmallMode	true	
User Comments		Instance-specific comments.

8.4.4 Instance cydff_4

Description: D Flip Flop with configurable reset and preset
Instance type: cydff [v1.30]
Datasheet: online component datasheet for cydff

Table 20. Component Parameters for cydff_4

Parameter Name	Value	Description
ArrayWidth	1	Width of d and q terminals. Must be between 1 and 32.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
MultiPresetReset	true	Defines options to set the preset and reset to be either a bus or a single bit.
PresetOrReset	None	Preset/ Reset parameter
SmallMode	true	
User Comments		Instance-specific comments.

8.4.5 Instance cydff_5

Description: D Flip Flop with configurable reset and preset
Instance type: cydff [v1.30]
Datasheet: online component datasheet for cydff

Table 21. Component Parameters for cydff_5

Parameter Name	Value	Description
ArrayWidth	1	Width of d and q terminals. Must be between 1 and 32.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
MultiPresetReset	true	Defines options to set the preset and reset to be either a bus or a single bit.
PresetOrReset	None	Preset/ Reset parameter
SmallMode	true	
User Comments		Instance-specific comments.

8.5 Component type: CyStatusReg [v1.90]

8.5.1 Instance Trigger_Status_Reg

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 22. Component Parameters for Trigger_Status_Reg

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Interrupt	false	Shows the interrupt terminal

Parameter Name	Value	Description
MaskValue	0	Defines the value of the interrupt mask
NumInputs	2	Defines the number of status inputs (1-8)
User Comments		Instance-specific comments.

8.6 Component type: Em_EEPROM [v2.20]

8.6.1 Instance On_Chip_EEPROM

Description: Emulates an EEPROM device in flash memory.
Instance type: Em_EEPROM [v2.20]
Datasheet: online component datasheet for Em_EEPROM

Table 23. Component Parameters for On_Chip_EEPROM

Parameter Name	Value	Description
Config Data in Flash	false	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
EEPROM Size	1024	Sets size of EEPROM. The size is rounded up to a full EEPROM page size.
Redundant Copy	No	If selected, then an 8-bit checksum is calculated on each row of data (that checksum is stored in the row), and a redundant copy of the row is stored in another location. When data is read the checksum is checked first. If the checksum is bad the redundant copy is restored.
Use Blocking Write	No	When set to "Yes" blocking writes to flash will be used in the design. Otherwise non-blocking flash writes will be used.
Use Emulated EEPROM	Yes	Selects if Emulated EEPROM flash area or User flash will be used for EEPROM storage
User Comments		Instance-specific comments.
Wear Level Factor	4x	Selects how much wear leveling is required. The higher the factor the more flash is used, but the higher number of erase/write cycles can be done on the EEPROM. Multiply this number by the datasheet write endurance spec to determine max write cycles.

8.7 Component type: SCB_I2C_PDL [v2.0]

8.7.1 Instance I2C

Description: I2C (SCB) communications interface
Instance type: SCB_I2C_PDL [v2.0]

Datasheet: online component datasheet for SCB_I2C_PDL

Table 24. Component Parameters for I2C

Parameter Name	Value	Description
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Data Rate (kbps)	100	This parameter specifies the data rate in kbps. The actual data rate may differ from the selected data rate due to the available clock frequency and Component settings. The standard data rates are 100 (default), 400, and 1000 kbps. The range: 1-1000 kbps
Enable Clock from Terminal	false	This parameter allows choosing between an internally configured clock (by the component) or an externally configured clock (by the user) for the component operation
Enable Manual SCL Control	false	This parameter specifies the method of calculating the SCL low and high phase duty cycle as automatic or manual (only applicable for the master modes).
Enable SCL trigger output	false	Enables scl_trig signal which allows connecting the SCL to the trigger mux so that it can be monitored by a TCPWM.
Mode	Master	This parameter defines the I2C operation mode as: the slave, master or master-slave.
Show I2C Terminals	false	This parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pin components.
Use RX FIFO	false	This parameter defines if the RX FIFO capabilites are used. Usage of the RX FIFO reduces the possibility of clock stretching and interrupt overhead.
Use TX FIFO	false	This parameter defines if the TX FIFO capabilites are used. Usage of the TX FIFO reduces the possibility of clock stretching and interrupt overhead.
User Comments		Instance-specific comments.

8.8 Component type: SCB_SPI_PDL [v2.0]

8.8.1 Instance SPI_NeoPixel

Description: SPI (SCB) communications interface
Instance type: SCB_SPI_PDL [v2.0]

Datasheet: online component datasheet for SCB_SPI_PDL

Table 25. Component Parameters for SPI_NeoPixel

Parameter Name	Value	Description
Bit Order	MSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Data Rate (kbps)	2500	This parameter specifies the data rate in kbps. The actual data rate may differ based on the available clock frequency and component settings. This parameter has no effect if the Enable Clock From Terminal parameter is true. The range: 1-25000 kbps.
Deassert SS Between Data Elements	false	This parameter determines if individual data transfers are separated by the slave select de-selection.
Enable Clock from Terminal	false	This parameter provides a clock terminal to connect a clock outside the component.
Enable Input Glitch Filter	false	This parameter applies a digital 3-tap median filter to the SPI input lines.
Enable MISO Late Sampling	false	This option allows the master to sample the MISO signal by half of the SCLK period later (on the alternate serial clock edge). Late sampling addresses the round-trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master.
Interrupt	Internal	This parameter allows choosing between Internal and External placement of the Interrupt Component.
Mode	Master	This parameter specifies the mode of the SPI operation as: the slave or master.
Number of SS	1	This parameter determines the number of the slave-select lines. The slave has a single slave-select line. The master has up to 4 lines. The range: 1-4.

Parameter Name	Value	Description
Oversample	5	This parameter defines how many Component clocks are used to generate the SCLK period (only applicable for the master mode). When the oversample is even the first and second phase of the clock period are the same. Otherwise the first phase of the clock signal period is one component's clock cycle longer than the second phase. The range: 4-16 (MISO presents) and 2-16 (MISO is removed).
Remove MISO	true	This option allows a removal of the MISO pin from the SPI interface
Remove MOSI	false	This option allows a removal of the MOSI pin from the SPI interface.
Remove SCLK	true	This option allows a removal of the SCLK pin from the SPI interface.
RX Data Width	8	This option defines the width of a single data element for the RX direction in bits. This number must match with TX Word Width for all SPI sub-modes except National Semiconductor (Microwire). The range: 4-16.
RX Output	false	This parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA trigger input or left unconnected.
SCLK Free Running	false	This parameter allows the master to generate SCLK continually. It is useful when the master SCLK is connected to the slave device which uses it for functional operation rather than only the SPI functionality.
SCLK Mode	CPHA = 1, CPOL = 1	This parameter specifies the serial clock phase (CPHA) and polarity (CPOL) combination.
Show SPI Terminals	true	This parameter removes internal pins and expose signals to terminals. These terminals must be connected to the pins or SmartIO component.
SS0 Polarity	Active Low	This parameter defines the active polarity of the slave-select 0 signal as Active Low or Active High.

Parameter Name	Value	Description
Sub Mode	Motorola	This parameter specifies the sub-mode of the SPI as: Motorola, TI (Start Coincides), TI (Start Precedes), or National Semiconductor (Microwire
TX Data Width	8	This option defines the width of a single data element for the TX direction in bits. This number must match with RX Word Width for all SPI sub-modes except National Semiconductor (Microwire). The range: 4-16.
TX FIFO Level	63	This parameter determines the behavior of the signal that drives the TX FIFO Below Level interrupt source and TX trigger output as follows: the signal remains active until the number of data elements in the TX FIFO is less than the value of the TX FIFO level. For example, the TX FIFO has 0 data elements (empty) and the TX FIFO level is 7. The signal remains active until TX FIFO is loaded to contain 7 data elements. The range: 0 – 127 (when TX/RX Word Width <= 8), and 0 - 63 otherwise.
TX Output	true	This parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA trigger input or left unconnected.
User Comments		Instance-specific comments.

8.9 Component type: SCB_UART_PDL [v2.0]

8.9.1 Instance UART_Audio

Description: UART (SCB) communications interface
Instance type: SCB_UART_PDL [v2.0]
Datasheet: online component datasheet for SCB_UART_PDL

Table 26. Component Parameters for UART_Audio

Parameter Name	Value	Description
Baud Rate (bps)	9600	This parameter specifies the baud rate in bps. The actual baud rate may differ based on the available clock frequency and Component settings. Range: 1 - 1000000 bps.

Parameter Name	Value	Description
Bit Order	LSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Break Signal Bits	11	This parameter specifies the break width in bits. The range: 7-16.
Com Mode	Standard	This parameter defines the sub-mode of UART as: Standard, SmartCard or IrDA.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
CTS	false	This parameter enables the cts input.
Data Width	8 bits	This option defines the width of a single data element in bits. The range: 4-9.
Drop on Frame Error	false	This parameter determines if the data is dropped from the RX FIFO on a frame error event.
Enable Clock from Terminal	false	This parameter allows choosing between an internally configured clock (by the component) or an externally configured clock (by the user) for the component operation.
Enable Digital Filter	false	This parameter applies a digital 3-tap median filter to the UART input lines.
Interrupt	Internal	This parameter allows choosing between Internal and External placement of the Interrupt Component.
Oversample	12	This parameter defines how many Component clocks oversample the selected baud rate. The range: 8 - 16 (except IrDA mode). The oversample values are predefined for IrDA mode.
Parity	None	This parameter defines the functionality of the parity bit location in the transfer as None, Odd or Even.
RTS	false	This parameter enables the rts output.
RX Output	false	This parameter enables the RX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.

Parameter Name	Value	Description
Show UART Terminals	false	This parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Stop Bits	1	This parameter defines the number of stop bits.
TX Output	false	This parameter enables the TX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
TX/RX Mode	TX + RX	This parameter enables the receiver or transmitter functionality or both simultaneously.
TX-Enable	false	This parameter enables TX_EN output.
User Comments		Instance-specific comments.

8.9.2 Instance UART_Console

Description: UART (SCB) communications interface
Instance type: SCB_UART_PDL [v2.0]
Datasheet: online component datasheet for SCB_UART_PDL

Table 27. Component Parameters for UART_Console

Parameter Name	Value	Description
Baud Rate (bps)	115200	This parameter specifies the baud rate in bps. The actual baud rate may differ based on the available clock frequency and Component settings. Range: 1 - 1000000 bps.
Bit Order	LSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Break Detected	false	This parameter enables the RX break detection interrupt source to trigger the interrupt output.
Break Signal Bits	11	This parameter specifies the break width in bits. The range: 7-16.
Com Mode	Standard	This parameter defines the sub-mode of UART as: Standard, SmartCard or IrDA.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
CTS	false	This parameter enables the cts input.

Parameter Name	Value	Description
Data Width	8 bits	This option defines the width of a single data element in bits. The range: 4-9.
Drop on Frame Error	false	This parameter determines if the data is dropped from the RX FIFO on a frame error event.
Enable Clock from Terminal	false	This parameter allows choosing between an internally configured clock (by the component) or an externally configured clock (by the user) for the component operation.
Enable Digital Filter	false	This parameter applies a digital 3-tap median filter to the UART input lines.
Interrupt	External	This parameter allows choosing between Internal and External placement of the Interrupt Component.
Oversample	12	This parameter defines how many Component clocks oversample the selected baud rate. The range: 8 - 16 (except IrDA mode). The oversample values are predefined for IrDA mode.
Parity	None	This parameter defines the functionality of the parity bit location in the transfer as None, Odd or Even.
RTS	false	This parameter enables the rts output.
RX FIFO Above Level	false	This parameter enables the RX FIFO above-level interrupt source to trigger the interrupt output
RX FIFO Full	false	This parameter enables the RX FIFO full interrupt source to trigger the interrupt output
RX FIFO not Empty	true	This parameter enables the RX FIFO not-empty interrupt source to trigger the interrupt output.
RX FIFO Overflow	false	This parameter enables the RX FIFO overflow interrupt source to trigger the interrupt output.
RX FIFO Underflow	false	This parameter enables the RX FIFO underflow interrupt source to trigger the interrupt output.
RX Frame Error	false	This parameter enables the RX frame error interrupt source to trigger the interrupt output.
RX Output	false	This parameter enables the RX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.

Parameter Name	Value	Description
Show UART Terminals	false	This parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Stop Bits	1	This parameter defines the number of stop bits.
TX FIFO Below Level	false	This parameter enables the TX FIFO below-level interrupt source to trigger the interrupt output.
TX FIFO Empty	false	This parameter enables the TX FIFO empty interrupt source to trigger the interrupt output.
TX FIFO not Full	false	This parameter enables the TX FIFO not-full interrupt source to trigger the interrupt output.
TX FIFO Overflow	false	This parameter enables the TX FIFO overflow interrupt source to trigger the interrupt output.
TX FIFO Underflow	false	This parameter enables the TX FIFO underflow interrupt source to trigger the interrupt output.
TX Output	false	This parameter enables the TX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
TX/RX Mode	TX + RX	This parameter enables the receiver or transmitter functionality or both simultaneously.
TX-Enable	false	This parameter enables TX_EN output.
UART Done	false	This parameter enables the UART done interrupt source to trigger the interrupt output.
User Comments		Instance-specific comments.

8.10 Component type: TCPWM_Counter_PDL [v1.0]

8.10.1 Instance Bit_Stream_Timer

Description: This component implements a Timer/Counter using the TCPWM hardware block
Instance type: TCPWM_Counter_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_Counter_PDL

Table 28. Component Parameters for Bit_Stream_Timer

Parameter Name	Value	Description
Capture Input	Disabled	This parameter determines if a Capture terminal is displayed on the schematic
Clock Prescaler	Divide by 1	Divides down the input clock
Compare or Capture	Capture	Selects the mode for the compare capture register

Parameter Name	Value	Description
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Direction	Up	Selects the direction the counter counts
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Interrupt Source	Overflow/Underflow	Selects which events can trigger an interrupt
Period	32768	Sets the period of the Timer/Counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Resolution	16-bits	Selects the size of the counter
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Stop Input	Disabled	Determines if a stop input is needed and how that input is registered
User Comments		Instance-specific comments.

8.10.2 Instance Local_Tag_Sensor_Bit_Stream_Timer

Description: This component implements a Timer/Counter using the TCPWM hardware block
Instance type: TCPWM_Counter_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_Counter_PDL

Table 29. Component Parameters for Local_Tag_Sensor_Bit_Stream_Timer

Parameter Name	Value	Description
Capture Input	Disabled	This parameter determines if a Capture terminal is displayed on the schematic
Clock Prescaler	Divide by 1	Divides down the input clock
Compare or Capture	Capture	Selects the mode for the compare capture register
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Direction	Up	Selects the direction the counter counts
Count Input	Disabled	Determines if a count input is needed and how that input is registered

Parameter Name	Value	Description
Interrupt Source	Overflow/Underflow	Selects which events can trigger an interrupt
Period	500000	Sets the period of the Timer/Counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Resolution	32-bits	Selects the size of the counter
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Stop Input	Disabled	Determines if a stop input is needed and how that input is registered
User Comments		Instance-specific comments.

8.10.3 Instance Local_Tag_Sensor_Bit_Stream_Timer_1

Description: This component implements a Timer/Counter using the TCPWM hardware block
Instance type: TCPWM_Counter_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_Counter_PDL

Table 30. Component Parameters for Local_Tag_Sensor_Bit_Stream_Timer_1

Parameter Name	Value	Description
Capture Input	Disabled	This parameter determines if a Capture terminal is displayed on the schematic
Clock Prescaler	Divide by 1	Divides down the input clock
Compare or Capture	Capture	Selects the mode for the compare capture register
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Direction	Up	Selects the direction the counter counts
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Interrupt Source	Overflow/Underflow	Selects which events can trigger an interrupt
Period	500000	Sets the period of the Timer/Counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered

Parameter Name	Value	Description
Resolution	32-bits	Selects the size of the counter
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Stop Input	Disabled	Determines if a stop input is needed and how that input is registered
User Comments		Instance-specific comments.

8.10.4 Instance Remote_Tag_Sensor_Bit_Stream_Timer

Description: This component implements a Timer/Counter using the TCPWM hardware block
Instance type: TCPWM_Counter_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_Counter_PDL

Table 31. Component Parameters for Remote_Tag_Sensor_Bit_Stream_Timer

Parameter Name	Value	Description
Capture Input	Disabled	This parameter determines if a Capture terminal is displayed on the schematic
Clock Prescaler	Divide by 1	Divides down the input clock
Compare or Capture	Capture	Selects the mode for the compare capture register
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Direction	Up	Selects the direction the counter counts
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Interrupt Source	Overflow/Underflow	Selects which events can trigger an interrupt
Period	500000	Sets the period of the Timer/Counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Resolution	32-bits	Selects the size of the counter
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered

Parameter Name	Value	Description
Stop Input	Disabled	Determines if a stop input is needed and how that input is registered
User Comments		Instance-specific comments.

8.11 Component type: TCPWM_PWM_PDL [v1.0]

8.11.1 Instance PWM_IR_Modulation

Description: This component implements a PWM using the TCPWM hardware block
Instance type: TCPWM_PWM_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_PWM_PDL

Table 32. Component Parameters for PWM_IR_Modulation

Parameter Name	Value	Description
Clock Prescaler	Divide by 1	Divides down the input clock
Compare 0	157	Sets the compare value. When the count value equals the compare the compare output pulses high. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Enable Compare Swap	false	When selected the compare register is swapped between compare 0 and compare 1 on the next OV/UN after the swap is registered
Enable Period Swap	false	If checked the periods will be swapped at the next OV/UN when a swap event has been registered
Interrupt Source	None	Selects which events can trigger an interrupt
Invert PWM Output	false	If checked the main PWM output is inverted
Invert PWM_n Output	false	If checked the main PWM_n output is inverted
Kill Input	Disabled	Determines how the kill input behaves
Kill Mode	Stop on Kill	Determines what the kill signal does to the PWM
Period 0	314	Sets the period of the counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
PWM Alignment	Left Aligned	Selects which direction the PWM counts in. Left = Up, Right = Down, Center/Asymmetric = Up/Down

Parameter Name	Value	Description
PWM Mode	PWM	Selects the PWM mode of operation
PWM Resolution	16-bits	Selects the width of the PWM
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Swap Input	Disabled	This input controls when compare and period swaps occur
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 6 register map is covered in the PSoC 6 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 6 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 6 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines